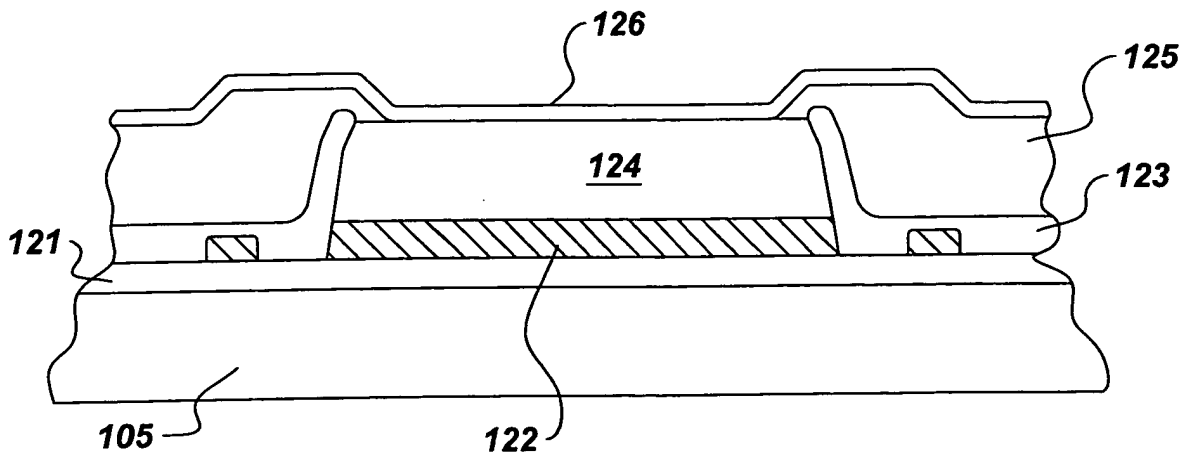
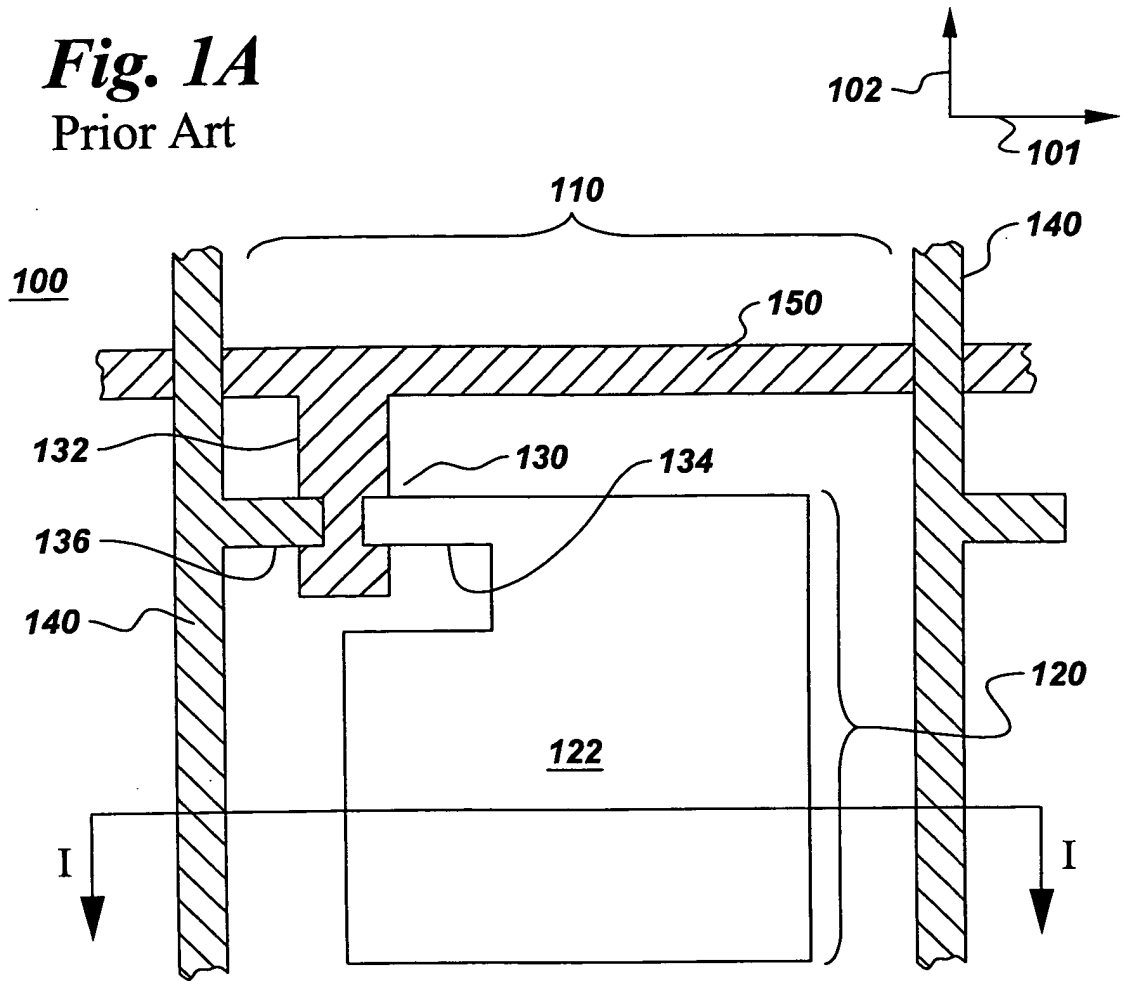


**Fig. 1A**  
Prior Art

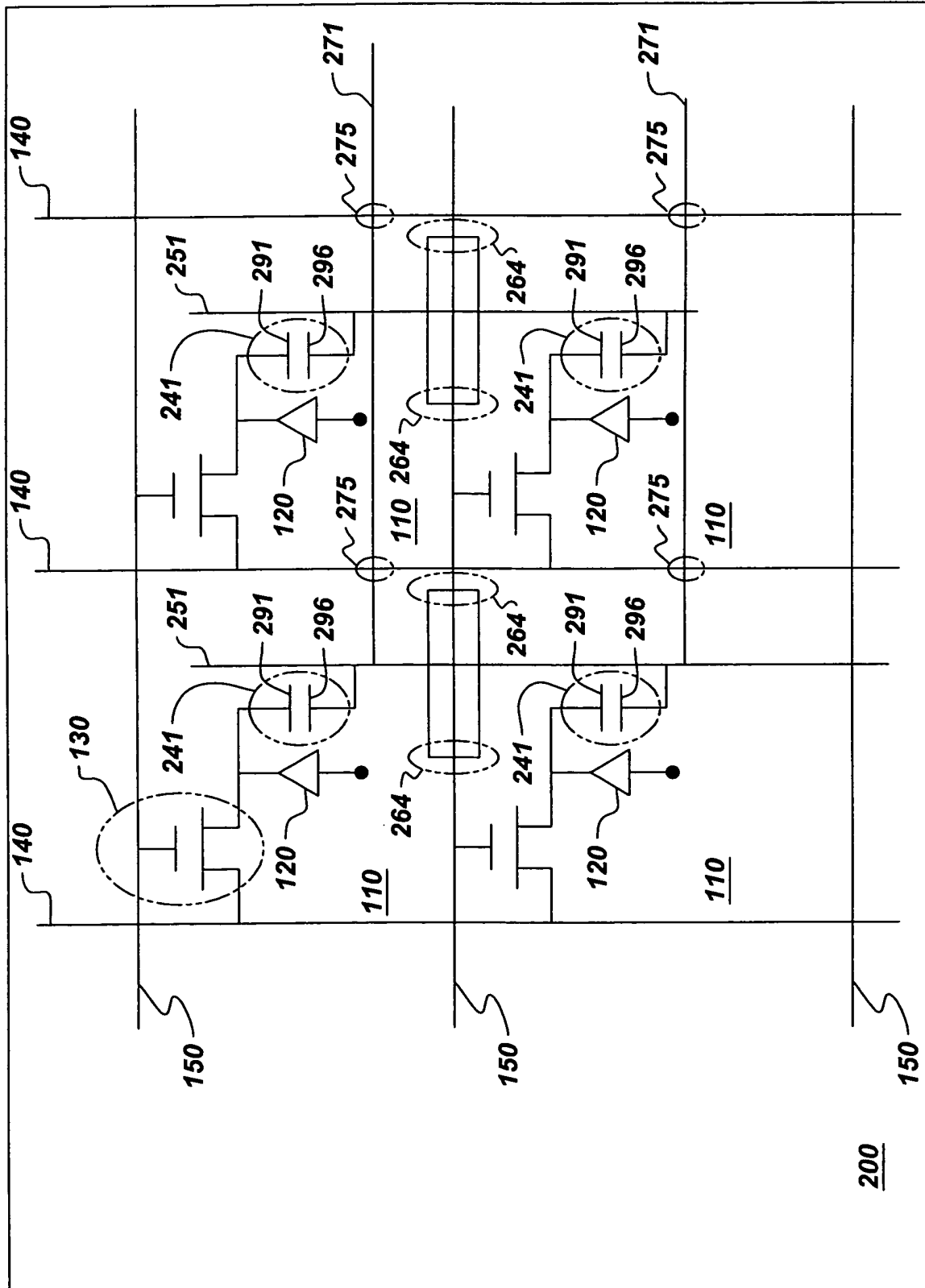


**Fig. 1B**  
Prior Art

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Figure 1 is a schematic diagram of a semiconductor device 100. The device consists of a 3x3 array of unit cells. Each unit cell contains a transistor 110. The transistor 110 has a gate 120 and a source/drain region 130. The array is defined by word lines 140 and bit lines 150. The top-left unit cell is further detailed with labels 132, 134, and 136 pointing to specific regions of the transistor. The entire array is enclosed within a dashed boundary 140. The device is labeled 100 at the bottom right.

**Fig. 2** Prior Art



**Fig. 3**